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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/551,027	04/17/2000	Wendell P. Noble	303.379US2	1158

21186 7590 09/04/2003

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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/551,027	NOBLE ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication app ars on the cov r sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *24* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed on December 31, 2002. Claims 20-56 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 20,21,23-25,27-28,30,32,34,35,37,39,41,42,44,46,48-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Gotou (5,001,526).

Gotou teaches a method for forming a semiconductor device comprising at least the steps of: forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein the access transistor includes, in order, a first source/drain region (68 in Fig 2, col 2, lines 11-54; or 15 in Fig 15b), a unitary body region (73 in Fig 2; or 14/16 in Figs 15b) and a second source/drain region formed vertically thereon (68,73,67 in Fig 2; cols 4-6); forming a trench capacitor, wherein a first plate (68 in Fig 2) of the capacitor is integral with the first source/drain region 15 or 68, wherein a second plate (69 in Fig 2; or 21 in Fig 3b,10,11a-b, re claim 21) surround the first plate forming a grid pattern (Figs 2,9a-b,11a-b,14a-b; re claim 23) by depositing polysilicon in row and column trenches (col 5, lines 22+); forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines (63 in Fig 2) with a gate of each word line interconnecting alternative access transistors on opposite sides of the trenches; and forming a number of bit lines 29 (figs 1) that interconnect second source/drain regions 17 of selected access transistors, wherein the memory device having an array of memory cells occupying an area of $4F^2$ with F is a minimum feature size (Fig 1; cols 1-2; col 2, lines 60-65, wherein the layers are epitaxially grown from a single silicon substrate wafer. Re further claims 25-26, epitaxially forming layers and etching the layers to form column bars of a first source/drain region, the body region, and the second source/drain region, and row and column isolation trenches are described from figures 6 to 14b (Fig 2; col 2, lines 11-54), and filling the trenches with a conductive material not to exceed the lower level of the body region 16 is shown in figure 15b, and wherein bit lines to interconnect the second source/drain regions is shown in

figures 14a-14b, wherein the first source/drain region extending outwardly from the substrate, and wherein the substrate is a single unbonded substrate.

Regarding the added limitation of wherein the trench capacitor is formed directly on the single unbonded substrate thus "without forming an implanted isolation region 70 in the substrate": First, Gotou teaches to form an implanted isolation region 70 (Fig 2) in the substrate. Second, Gotou discloses to form the "implanted isolation region" 70 in the substrate 60 to eliminate leakage of electric charges between adjacent storage electrodes (col 2, lines 33-43; Fig 2). Gotou thus already recognizes and discloses that "without forming an implanted isolation region in the substrate', the leakage of electric charges between adjacent storage electrodes is not eliminated. Accordingly, Gotou is still outstanding under 35 USC 102 anticipation although teach way from that limitation, wherein by not forming the implanted isolation region 70, the trench capacitor is formed directly on the single unbonded substrate.

2. Claims 20,21,23-25,27-28,30,32,34,35,37,39,41,42,44,46,48-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (EP 0 198 590).

Wada teaches a method for forming a semiconductor device comprising at least the steps of: forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein the access transistor includes, in order, a first source/drain region 20 (Fig 2; col 5, lines 10-36), a unitary body region 26 and a second source/drain region 32 formed vertically thereon; forming a trench capacitor, wherein a first plate (Figs 2-3; col 5, line 30 through col 7) of the capacitor is integral with the first source/drain region 20, wherein a second plate 22 surround the first plate forming a grid pattern (Figs 2,3,5) by depositing a polysilicon layer in row and column trenches (col 9, lines 5-49); forming a number of word lines 66'in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines (66' in Figs 4E-4F) with a gate of each word line interconnecting alternative access transistors on opposite sides of the trenches; and forming a number of bit lines that interconnect second source/drain regions of selected access transistors, wherein the memory device having an array of memory cells occupying an area of $4F^2$ with F is a minimum feature size (Fig 5), wherein the silicon layer 50 is epitaxially grown from a single silicon substrate wafer (Fig 4A, col 7, lines 37-44). Re further claims 25-

26, epitaxially forming layers and etching the layers to form column bars of a first source/drain region, the body region, and the second source/drain region, and row and column isolation trenches are described from figures 4A-4G, and filling the trenches with a conductive material not to exceed the lower level of the body region is shown in figure 4E, and wherein bit lines to interconnect the second source/drain regions is shown in figures 1, 4 and 5, wherein the first source/drain region extending outwardly from the substrate, and wherein the substrate is a single unbonded substrate.

Claim Rejections - 35 USC § 103

3. Claims 20,21,23-25,27-28,30,32,34,35,37,39,41,42,44,46,48-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotou (5,001,526) taken with Joyner et al (5,429,955) and Wada (EP 0 198 590).

Gotou teaches a method for forming a semiconductor device comprising at least the steps of: forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein the access transistor includes, in order, a first source/drain region (68 in Fig 2, col 2, lines 11-54; or 15 in Fig 15b), a unitary body region (73 in Fig 2; or 14/16 in Figs 15b) and a second source/drain region formed vertically thereon (17 in Fig 3b; or 68,73,67 in Fig 2; cols 4-6); forming a trench capacitor, wherein a first plate (15 in Fig 3b; or 68 in Fig 2) of the capacitor is integral with the first source/drain region 15 or 68, wherein a second plate (69 in Fig 2; or 21 in Fig 3b,10,11a-b, re claim 21) surround the first plate forming a grid pattern (Figs 2,3a-b,9a-b,11a-b,14a-b; re claim 23) by depositing polysilicon in row and column trenches (col 5, lines 22+); forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines (30 in Fig 3b; or 63 in Fig 2) with a gate of each word line interconnecting alternative access transistors on opposite sides of the trenches; and forming a number of bit lines 29 (figs 3b, 1,14a-b) that interconnect second source/drain regions 17 of selected access transistors, wherein the memory device having an array of memory cells occupying an area of $4F^2$ with F is a minimum feature size (Fig 14a,11a,1; cols 1-2; col 2, lines 60-65, wherein the layers are epitaxially grown from a single silicon substrate wafer. Re further claims 25-26, epitaxially forming layers and etching the layers to form column bars of a first source/drain region, the body region, and the second source/drain region, and row and column

isolation trenches are described from figures 6 to 14b (or Fig 2; col 2, lines 11-54), and filling the trenches with a conductive material not to exceed the lower level of the body region 16 is shown in figure 15b, and wherein bit lines to interconnect the second source/drain regions is shown in figures 14a-14b, wherein the first source/drain region extending outwardly from the substrate.

Gotou provides a single bonded substrate for forming transistors; whereas, the present claimed invention recites "unbonded substrate".

However, Joyner et al teaches (at col 2, lines 20-30; col 3, Figs 1-3) to use a single SOI implanted-oxygen substrate instead of using the bonded substrate (col 1). Wada teaches forming the trench capacitor on the silicon substrate (Figs 2-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Gotou by implant oxygen into a substrate instead of bonding two substrates as taught by Joyner. This is because of the desirability to eliminate or reduces disadvantages of having limitations on the minimum thickness and the uniformity, and voiding problems. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench capacitor directly on the silicon substrate as taught by Wada or with an isolation region between the trench capacitor and the silicon substrate as taught by Gotou, because these structure are alternative for substitution, wherein leakage of electrical charge is eliminated by including the isolation region, and wherein processing step is reduced by not including the isolation region.

4. Claims 22,26,29,31,33,36,38,40,43,45,47,54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotou (5,001,526) with Joyner et al (5,429,955) and/or Wada (EP 0 198 590), as applied above, taken with Kimura et al (5,177,576).

Gotou and Joyner teaches a method for forming a memory array as applied above to claims 20,21,23-25,27-28,30,32,34,35,37,39,41,42,44,46,48-53. Wada teaches a method for forming a memory array as applied above to claims 20,21,23-25,2728,30,32,34,35, 37,39, 41,42,44,46, and 48-53.

Re claim 22, Gotou or Wada lacks to form a contact to couple the second plate to an underlying semiconductor layer. Re claims 29,31,33,36,38,40,43,45,47, Gotou or Wada lacks to

mention claimed thickness of the source/drain regions. Re claims 54-55, Gotou or Wada teaches DRAM memory cells but lacks to explicitly mention about decoder, buffer and microprocessor.

However, re claim 22, Kimura et al teach (at fig 4, figs 6G-6M; col 6, lines 30-68) to form a contact at the bottom of the trench so that the contact couples a second plate to an underlying semiconductor layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a contact at the bottom of the trench so that the contact couples a second plate to an underlying semiconductor layer, as taught by Kimura because of the desirability to form an electrical connection between the second plate and the semiconductor wafer, wherein forming the contact directly at the bottom of trench for connection would miniaturize a device size.

Re claims 54-55, it would have been obvious to one of ordinary skill in the art to connect bit lines and word lines of the DRAM memory cells to decoders, buffers and microprocessor as well known in the art because of the desirability to provide the capability of accessing a charged stored in one or more of the capacitors or providing a charge thereto (read/write).

Re claims 29,31,33,36,38,40,43,45,47, it would have been to one of ordinary skill in the art to select a thickness value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233. Normally, it is to be expected that a change in thickness, depth, etc., or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from results of prior art...such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality. *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In Re Irmscher* 166 USPQ 314 (CCPA 1945); *In Re Norman* 66 USPQ 308 (CCPA 1945); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

Response to Arguments

5. Applicant's amendment and convincing remarks that Ho et al (4,252,579) do not teaches each of the trenches including two word lines. Accordingly, rejection using Ho is withdrawn.

6. Applicant's other remarks filed December 31, 2003 have been fully considered but they are not persuasive and in moot of new ground of rejection.

** Regarding 35 USC 102 Rejection using Gotou (5,001,526): Applicant remarked that Figure 2 of Gotou shows an isolation region 70 formed between the capacitor and the substrate.

In response, it is not disagreed with Applicant that the isolation region 70 is shown in Figure 2. However, it is alleged that Gotou discloses forming the "implanted isolation region" 70 in the substrate 60 so as to eliminate leakage of electric charges between adjacent storage electrodes (col 2, lines 33-43; Fig 2). Gotou thus already recognizes and discloses that "without forming an implanted isolation region in the substrate', the leakage of electric charges between adjacent storage electrodes is not eliminated. Accordingly, by not forming the implanted isolation region 70, the trench capacitor is formed directly on the single unbonded substrate. Gotou is still outstanding under 35 USC 102 anticipation although teach way from that limitation. As can be seen, Wada teaches forming the trench capacitor directly on the silicon substrate without forming an isolation region between the capacitor and the substrate.

** Regarding 35 USC 103 rejections using Gotou with Joyner, and/or Wada and further of Kimura: The combination of Gotou and Joyner prima facie obviously establishes the invention as claimed, wherein Joyner clearly teaches to provide an SOI wafer by using a single SOI implanted oxygen substrate instead of using the singly unbonded substrate. The rejection is still outstanding even though the prior art references included other processing steps, which processing steps are not included in the claims, or not claimed by the claimed invention.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

oacs

Michael Trinh
Primary Examiner